Jianlei Yang

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RESEARCH INTERESTS

- Energy-efficient computing platforms for deep learning and machine vision
- Non-volatile memory design and neuromorphic computing systems
- Numerical algorithms for large scale integrated circuit simulation

EDUCATION

09/2009 - 07/2014 **PhD** in Department of Computer Science and Technology
Tsinghua University, Beijing, China
Thesis: *On-Chip Power Supply Network Simulation and Verification for Large Scale Integrated Circuits* (with honors), Advisor: Prof. **Yici Cai**.

09/2005 - 07/2009 **B.S.** in Microelectronics, **Xidian University**, Xi'an, China

PROFESSIONAL EXPERIENCES

02/2016 - Present **Associate Professor** in School of Computer Science and Engineering
Beihang University, Beijing, China.

11/2014 - 01/2016 **Postdoctoral Researcher** in Evolutionary Intelligence Laboratory
University of Pittsburgh, Pittsburgh, Pennsylvania, USA.
Research topics: Robust STT-MRAM design and neuromorphic computing with crossbar structures, working with **Prof. Hai (Helen) Li** and **Prof. Yiran Chen**.

07/2013 - 07/2014 **Research Intern**, Embeded Architecture Group in **Intel Labs China**, Beijing, China.
Projects: SOC power modeling and dynamic time warping (DTW) techniques.

07/2012 - 08/2012 **Research Intern**, Nimbus Automation Technologies, Shanghai, China.
Projects: Physical design techniques in the cloud computing systems.

SELECTED RESEARCH CONTRIBUTIONS

1. *Early Stage Simulation of On-Chip Power Grid*: Developed efficient solvers for large scale power grid simulation on early design stage, by introducing a fast Poisson solver as an analytical preconditioner for iterative solvers to speedup the simulation [ICCAD'2011, TVLSI'2014]. My work demonstrates about 20X speedups when grid locality is exploited for quasi-Poisson block.
2. *Static Simulation of On-Chip Power Grid*: Developed efficient linear solvers for static analysis of power grid, by introducing an aggregation based algebraic multigrid preconditioned conjugate gradient method to speedup the DC simulation [ICCAD'2011, TAU'2012, TVLSI'2014]. The proposed solver *PowerRush* achieves about tens of speedups than other widely used solvers, and won the first place in the first annual power grid simulation contest on TAU workshop 2011. The contest results show that *PowerRush* not only has a better solving efficiency but also is extremely memory efficient (using only about 40% runtime and 75% memory respectively compared with the second place performance of other simulators).
3. *Transient Simulation of On-Chip Power Grid*: Developed an efficient transient simulator for large scale RLC network [ICCAD'2012], and won the second place in the transient power grid simulation contest on TAU workshop 2012. The contest results show that our proposed simulator is still extremely efficient in memory consumption (with a memory footprint less than half of other teams).
4. *Vectorless Verification of Early Stage Power Grid*: Proposed several efficient vectorless power grid verification techniques for early stage safety check without input current patterns [ICCD'2013, ASPDAC'2013, ASPDAC'2014, TVLSI'2014] (received a Best Paper Award at ICCD'2013), which enables us to verify large scale power grid with uncertainty working mode.

5. *Neuromorphic Chip Design*: Lead a design team with more than 8 graduate students for neurocognitive chip designs, funded by DARPA and US AFRL. Very familiar with neuromorphic computing and achieving good design experiences in neurocognitive chip design as well as project and team management. Two crossbar-based neuromoorphic chips for pattern recognition have been successfully taped-out in November 2015 and February 2016.

REFEREED JOURNAL ARTICLES

1. **Jianlei Yang**, Xueyan Wang, Qiang Zhou, Zhaohao Wang, Hai (Helen) Li, Yiran Chen, Weisheng Zhao. *Exploiting Spin-Orbit Torque Devices as Reconfigurable Logic for Circuit Obfuscation*, to appear on IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018. (**TCAD**)
2. Yu Zhang, Xiaoyang Lin, JeanPaul Adam, Guillaume Agnus, Wang Kang, Wenlong Cai, JeanRene Coudevylle, Nathalie Isac, **Jianlei Yang**, Huaiwen Yang, Kaihua Cao, Hushan Cui, Deming Zhang, Youguang Zhang, Chao Zhao, Weisheng Zhao, Dafine Ravelosona. *Heterogeneous Memristive Devices Enabled by Magnetic Tunnel Junction Nanopillars Surrounded by Resistive Silicon Switches*, Advanced Electronic Materials, 2018. (**AEM**)
3. Lin Feng, Shuzhang Liang, Xiangcong Zhou, **Jianlei Yang**, Yonggang Jiang, Deyuan Zhang, Fumihito Arai. *On-chip microfluid induced by oscillation of microrobot for noncontact cell transportation*, Applied Physics Letters, 111, 203703, 2017. (**APL**)
4. Bi Wu, Yuanqing Cheng, **Jianlei Yang**, Aida Todri-Sanial and Weisheng Zhao. *Temperature Impact Analysis and Access Reliability Enhancement for 1T1MTJ STT-RAM*, IEEE Transactions on Reliability, vol. 65, no. 4, pp. 1755-1768, 2016. (**TR**)
5. Yuanqing Cheng, Aida Todri-Sanial, **Jianlei Yang** and Weisheng Zhao. *Alleviating Through Silicon Via Electromigration for Three-dimensional Integrated Circuits Taking Advantage of Self-healing Effect*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 11, pp. 3310-3322, 2016. (**TVLSI**)
6. **Jianlei Yang**, Zhenyu Sun, Xiaobin Wang, Yiran Chen, Hai (Helen) Li. *Spintronic Memristor as Interface between DNA and Solid State Devices*, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 6, no. 2, pp. 212-221, 2016. (**JETCAS**)
7. **Jianlei Yang**, Peiyuan Wang, Yaojun Zhang, Yuanqing Cheng, Weisheng Zhao, Yiran Chen, Hai (Helen) Li. *Radiation-Induced Soft Error Analysis of STT-MRAM: A Device to Circuit Approach*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 3, pp. 380-393, 2016. (**TCAD**)
8. **Jianlei Yang**, Yici Cai, Qiang Zhou, Wei Zhao. *A Selected Inversion Approach for Locality Driven Vectorless Power Grid Verification*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 11, pp. 2617-2628, 2015. (**TVLSI**)
9. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: An Efficient Simulator for Static Power Grid Analysis*. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 10, pp. 2103-2116, 2014. (**TVLSI**)
10. **Jianlei Yang**, Yici Cai, Qiang Zhou, Jin Shi. *Friendly Fast Poisson Solver Preconditioning Technique for Power Grid Analysis*. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 4, pp. 899-912, 2014. (**TVLSI**)

REFEREED CONFERENCE PAPERS

11. Xiaotao Jia, **Jianlei Yang**, Zhaohao Wang, Yiran Chen, Hai (Helen) Li, Weisheng Zhao, *Spintronics based Stochastic Computing for Efficient Bayesian Inference System* , Proceedings of IEEE 23th Asia and South Pacific Design Automation Conference, Jeju, 2018. (**ASP-DAC**)
12. Chenguang Wang, Ming Yan, Yici Cai, Qiang Zhou, **Jianlei Yang**, *Power Profile Equalizer: A Lightweight Countermeasure against Side-channel Attack*, Proceedings of IEEE/ACM International Conference on Computer Design, pp. 305-312, Boston, 2017. (**ICCD**)
13. Bi Wu, Yuanqing Cheng, Pengcheng Dai, **Jianlei Yang**, Youguang Zhang, Dijun Liu, Ying Wang, Weisheng Zhao, *Thermosiphon: A Thermal Aware NUCA Architecture for Write Energy Reduction of the STT-MRAM based LLCs*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 474-481, Irvine, 2017. (**ICCAD**)
14. Jinglan Liu, Yukun Ding, **Jianlei Yang**, Ulf Schlichtmann, Yiyu Shi, *Generative adversarial network based scalable on-chip noise sensor placement*, Proceedings of 30th IEEE International System-on-Chip Conference, pp. 239-242, Munich, 2017. (**SoCC**)

15. Zhiyao Gong, Keni Qiu, Weiwen Chen, Yuanhui Ni, Yuanchao Xu, **Jianlei Yang**, *Pipeline Optimizations of Architecting STT-RAM as Registers in Rad-Hard Environment*, Proceedings of IEEE International Conference on Embedded Software and Systems, pp. 844-852, Sydney, 2017. (**ICESS Best Paper Award**)
16. Xueyan Wang, Xiaotao Jia, Qiang Zhou, Yici Cai, **Jianlei Yang**, Mingze Gao, Gang Qu, *Secure and Low-Overhead Circuit Obfuscation Technique with Multiplexers*, Proceedings of ACM Great Lakes Symposium on VLSI, pp. 133-136, Boston, 2016. (**GLSVLSI**)
17. Linuo Xue, Yuanqing Cheng, **Jianlei Yang**, Peiyuan Wang, Yuan Xie, *ODESY: a novel 3T-3MTJ cell design with optimized area DEnsity, scalability and latencY*. Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 118, Austin, 2016. (**ICCAD**)
18. Chenchen Liu, Qing Yang, Bonan Yan, **Jianlei Yang**, Xiaocong Du, Weijie Zhu, Hao Jiang, Qing Wu, Mark Barnell, Hai Li, *A Memristor Crossbar Based Computing Engine Optimized for High Speed and Accuracy*, Proceedings of IEEE Computer Society Annual Symposium on VLSI, pp. 110-115, Pittsburgh, 2016. (**ISVLSI**)
19. You Wang, Hao Cai, Lirida A. B. Naviner, Jacques-Olivier Klein, **Jianlei Yang**, Weisheng Zhao, *A novel circuit design of true random number generator using magnetic tunnel junction*, Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures, pp. 123-128, Beijing, 2016. (**NANOARCH**)
20. Zheng Li, Chenchen Liu, Yandan Wang, Bonan Yan, Chaofei Yang, **Jianlei Yang** and Hai (Helen) Li, *An overview on memristor crossabr based neuromorphic circuit and architecture*, Proceedings of IFIP/IEEE International Conference on Very Large Scale Integration, pp. 52-56, Daejeon, 2015. (**VLSI-SoC Invited Paper**)
21. Bonan Yan, Zheng Li, Yaojun Zhang, **Jianlei Yang**, Weisheng Zhao, Pierre Chor-Fung Chia and Hai (Helen) Li. *A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback*, Proceedings of ACM Great Lakes Symposium on VLSI, pp. 69-74, Pittsburgh, 2015. (**GLSVLSI Best Paper Nomination**)
22. **Jianlei Yang**, Liwei Ma, Kang Zhao, Yici Cai, Tin-Fook Ngai. *Early Stage Real-Time SoC Power Estimation Using RTL Instrumentation*, Proceedings of IEEE 20th Asia and South Pacific Design Automation Conference, pp. 779-784, Chiba/Tokyo, 2015. (**ASP-DAC**)
23. **Jianlei Yang**, Chenguang Wang, Yici Cai, Qiang Zhou. *Power Supply Noise Aware Evaluation Framework for Side Channel Attacks and Countermeasures*, Proceedings of IEEE International Conference on Field-Programmable Technology, pp. 161-166, Shanghai, 2014. (**FPT Invited Paper** by Special Session of Hardware Security).
24. Wei Zhao, Yici Cai, **Jianlei Yang**. *Fast Vectorless Power Grid Verification using Maximum Voltage Drop Location Estimation*, Proceedings of IEEE 19th Asia and South Pacific Design Automation Conference, pp. 861-866, Singapore, 2014. (**ASP-DAC**)
25. **Jianlei Yang**, Yici Cai, Qiang Zhou, Wei Zhao. *Selected Inversion for Vectorless Power Grid Verification by Exploiting Locality*, Proceedings of IEEE International Conference on Computer Design, pp. 257-263, Asheville, 2013. (**ICCD Best Paper Award**)
26. Wei Zhao, Yici Cai, **Jianlei Yang**. *A multilevel H-matrix-based approximate matrix inversion algorithm for vectorless power grid verification*, Proceedings of IEEE 18th Asia and South Pacific Design Automation Conference, pp. 163-168, Yokohama, 2013. (**ASP-DAC**)
27. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: Efficient transient simulation for power grid analysis*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 653-659, San Jose, 2012. (**ICCAD Invited Paper** by Special Session of Power grid simulation and verification for billion-transistor VLSI designs)
28. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: A linear simulator for power grid*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 482-487, San Jose, 2011. (**ICCAD Invited Paper** by Special Session of 2011 TAU Power Grid Contest)
29. **Jianlei Yang**, Yici Cai, Qiang Zhou, Jin Shi. *Fast Poisson solver preconditioned method for robust power grid analysis*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 531-536, San Jose, 2011. (**ICCAD**)
30. Feifei Niu, Qiang Zhou, Hailong Yao, Yici Cai, **Jianlei Yang**, Chin Ngai Sze. *Obstacle-avoiding and slew-constrained buffered clock tree synthesis for skew optimization*, Proceedings of ACM Great Lakes Symposium on VLSI, pp. 199-204, Lausanne, 2011. (**GLSVLSI**)

WORKSHOP PAPERS

31. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: A Linear Simulator for Power Grid*, IEEE/ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, Taipei, 2012. (**TAU Invited Paper**)

PATENTS

1. Yici Cai, Qiang Zhou, **Jianlei Yang**, *A Transient Simulation Method for On-Chip Power Grid with RCL Network*, Apply Number: 201310152859.X, Apply Date: 2013-04-27, Public Number: 103207941A, Public Date: 2013-07-17.
2. Yici Cai, Qiang Zhou, **Jianlei Yang**, Zuowei Li, *A Simulation Method for On-Chip Power Grid*, Apply Number: 201210073172.2, Apply Date: 2012-03-19, Public Number: 102663166A, Public Date: 2012-09-12.
3. Qiang Zhou, Yici Cai, Zuowei Li, **Jianlei Yang**, *A Construction Method of Conductance Matrix for On-Chip Power Grid Simulation*, Apply Number: 201210058929.0, Apply Date: 2012-03-07, Public Number: 102646143A, Public Date: 2012-08-22.
4. Qiang Zhou, Yici Cai, Zuowei Li, **Jianlei Yang**, *An Adaptive Method of Handling Metal Vias for On-Chip Power Grid Simulation*, Apply Number: 201210058540.6, Apply Date: 2012-03-07, Public Number: 102592033A, Public Date: 2012-07-18, Grant Date: 2013-07-24.
5. Yici Cai, Qiang Zhou, **Jianlei Yang**, *A Friendly Extraction Method of Specific Parasitic Devices for Analog Integrated Circuits*, Apply Number: 201010262309.X, Apply Date: 2010-08-25, Public Number: 1923595A, Public Date: 2010-12-22, Grant Date: 2012-10-24.

HONORS AND AWARDS

05/2015	**Best Paper Nomination**, ACM Great Leak Symposium on VLSI.
06/2014	**Outstanding Doctoral Dissertations Award**, Tsinghua University.
11/2013	Ranked as the top 5 teams, in ICCAD Contest 2013, topic: Detailed Placement.
10/2013	National Scholarship, Tsinghua University.
10/2013	**Best Paper Award**, IEEE International Conference on Computer Design, 2013.
10/2012	The IBM Chinese Excellent Student Scholarship.
01/2012	**Second Place**, in Power Grid Transient Simulation Contest on ACM/IEEE TAU Workshop Sponsored by IBM, with award of $600 from IBM, SpringSoft and TSMC.
04/2011	**First Place**, in Power Grid Simulation Contest on ACM/IEEE TAU Workshop Sponsored by IBM, with award of $600.
10/2011	Kwang-Hua Scholarship, First Class, Tsinghua University.
10/2008	National Endeavor Scholarship, Xidian University.
02/2008	Meritorious Winner (First Prize), in Mathematical Contest on Modeling (MCM) by COMAP, U.S.A., Paper Title: When Sudoku Comes across Information Theory.

RESEARCH PROJECT EXPERIENCES

1. An Adaptive Information Processing System Resilient to Device Variations and Noises
   Sponsored by *Defense Advanced Research Projects Agency (DARPA)*. (2014-present)
2. Neuromorphic Computing Engine with Resistive Crossbar Architecture
   Sponsored by *US Air Force Research Lab (AFRL)*. (2014-present)
3. Nonvolatile TCAM Circuit Design Based on Spintronic Technology
   Sponsored by *Cisco Systems, Inc.*. (2014-present)
4. Power Grid Network Analysis and Verification Techniques for Nanometer SoC Design
   Sponsored by *National Science Foundation of China*. (2013-2016)
5. Development and Application of EDA Platform and System
   Sponsored by *Important Specific Project in Kernel Electronic Devices, High-end General Application Chips and Fundamental Software Products*. (2011-2014)
6. Automatic Routing Techniques for Nanometer Integrated Circuits
   Sponsored by *National Science Foundation of China*. (2010-2012)
7. Efficient Simulation and Optimization Techniques for Large Scale On-Chip Power Grid Design
   Sponsored by *National Science Foundation of China*. (2008-2010)
8. Advanced EDA Platform Development
   Sponsored by *Important Specific Project in Kernel Electronic Devices, High-end General Application Chips and Fundamental Software Products*. (2008-2010)

TEACHING EXPERIENCES

- Teaching Assistant, *Numerical Analysis*, Prof. Yici Cai
  Undergraduate Course at Tsinghua University, Spring 2010, Spring 2012, Spring 2014
- Teaching Assistant, *Introduction to VLSI Design*, Prof. Yici Cai
  Undergraduate and Graduate Course at Tsinghua University
  Fall 2009, Fall 2010, Fall 2011, Fall 2012, Fall 2013, Fall 2014
- Teaching Assistant, *The Layout Theories and Algorithms for VLSI*, Prof. Qiang Zhou
  Graduate Course at Tsinghua University, Spring 2011, Spring 2013
- Teaching Assistant, *Design Automation for Digital Systems*, Prof. Qiang Zhou
  Undergraduate Course at Tsinghua University, Spring 2013
- Teaching Assistant, *Program Design and Training*, Prof. Hailong Yao
  Undergraduate Course at Tsinghua University, Summer 2012

PROFESSIONAL ACTIVITIES

Served as conference TPC member:

- IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), 2018.

Invited reviewer for top journals and conferences in VLSI/CAD:

- ACM/EDAC/IEEE Design Automation Conference (DAC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
- IEEE International Symposium on Quality Electronic Design (ISQED)
- Elsevier - Integration, the VLSI Journal

QUALIFICATIONS AND SKILLS

- Proficient in C/C++, Tcl/Tk, Linux Shell, Matlab, Python, Qt, Verilog HDL, HSPICE and LaTeX
- Skilled in EDA software development and OpenAccess API
- Skilled in using analog/digital system synthesis and physical design tools
- Skilled in analog-mixed signal circuit/chip design techniques
- English Proficiency Test of Tsinghua University II
- College English Test Band 4 (CET-4) & Test Band 6 (CET-6)

SERVICES

08/2012 & 07/2013	Student Local Host in Tsinghua for NSF-IRES Program Ceitres @ UC Riverside, Directed by Dr. Sheldon X.-D. Tan
05/2010 - 06/2014	System Administrator of Linux Servers at EDA Lab Dept. of Computer and Science Technology, Tsinghua University